

C. Remarks

The claims are 1-19, with claim 1 being the sole independent claim. Claim 1 has been amended to better define the present invention. Support for this amendment may be found throughout the specification and in Figs. 1A-1H. Claims 3 and 15 have been amended to reflect the changes in claim 1. Reconsideration of the claims is expressly requested.

As a formal matter, Applicant has noted that the Examiner did not correctly indicate in the Office Action summary that a certified copy of the priority document has been received. Specifically, box (12)(a)(1) should be checked. An appropriate notification is requested in subsequent communications from the Office.

Claims 1-19 stand rejected under 35 U.S.C. 102(b) as being allegedly anticipated by U.S. Patent No. 6,191,007 B1 (Matsui). The grounds of rejection are respectfully traversed.

Prior to addressing the merits of rejection, Applicant would like to review some of the key features of the presently claimed invention. That invention is directed to a method for manufacturing a partial SOI substrate. This method includes a step of forming a first substrate, which has a semiconductor region, a partial insulating layer and a semiconductor layer. The semiconductor region includes first and second regions, and the partial insulating layer is arranged on the first region so as to be in contact with the first region. The semiconductor layer is arranged on the second region and the partial insulating layer. The method also includes a step of implanting ions into the first substrate through a surface of the first substrate to form a separation layer at a position deeper than a position

of the partial insulating layer. In addition, the method includes a step of bonding a second substrate to the surface of the first substrate in which the separation layer is formed, to form a bonded substrate stack. Furthermore, the method includes a step of splitting the bonded substrate stack at the separation layer to form a partial SOI substrate, which includes an SOI layer comprised of the first region arranged on the partial insulating layer so as to be in contact with the partial insulating layer.

Matsui is directed to a method for manufacturing a semiconductor substrate having a patterned structure to bury an electrode in a semiconductor layer. Matsui discloses forming a silicon oxide film 5 on an electrode pattern 3 and on a silicon oxide film 2, and then forming a polysilicon film 6 on the silicon oxide film 5.

The Examiner has alleged that the silicon oxide film 5 corresponds to the partial insulating layer of the present invention. Applicant respectfully disagrees.

Applicant submits that the silicon oxide film 5 in Matsui is quite different from the partial insulating layer of the present invention. Specifically, in the presently claimed invention, the semiconductor region includes the first and second regions, the partial insulating layer is arranged on the first region so as to be in contact with the first region, and the semiconductor layer is arranged on the second region and the partial insulating layer. In contrast, in Matsui, the silicon oxide film 5 is formed on the electrode pattern 3 and the silicon oxide film 2. Therefore, the silicon oxide film 5 is not formed on a semiconductor region such that the silicon oxide film 5 is in contact with the semiconductor region.

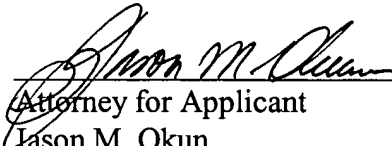
Accordingly, Applicant respectfully submits that Matsui fails to disclose or suggest forming a partial insulating layer, which is in contact with the first semiconductor

region. Consequently, the method taught by Matsui does not result in a structure of a partial SOI substrate in which an SOI layer comprises a first region arranged on and in contact with the partial insulating layer. Thus, the present claims are clearly patentable over Matsui.

Wherefore, Applicant respectfully requests that the outstanding rejection be withdrawn and that the present case be passed to issue.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address given below.

Respectfully submitted,



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/654,022

09/04/2003

Nobuhiko Sato

00862.023223

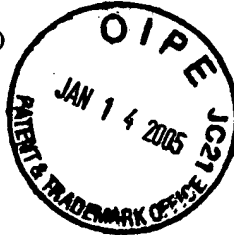
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NEW YORK, NY 10112



EXAMINER

TSAI, H JEY

ART UNIT

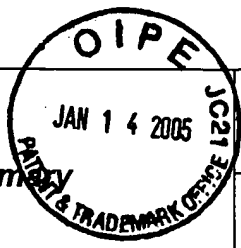
PAPER NUMBER

2812

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

FILE NO. 00862-023223
ATTORNEY PS
DUE DATE 4/5/05 - 5/10/05
DOCKETED 1/10/05 qu



Office Action Summary

Application No.

10/654,022

Applicant(s)

SATO ET AL.

Examiner

H.Jey Tsai

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 4-10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Election/Restriction

This application contains claims drawn to an invention nonelected claims. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishida et al. 5,403,771 or Takasu 5,402,989 or Koide et al. 6,617,668 in view of Short et al. 4,851,078, all are previously cited.

Hishida teaches a substrate manufacturing method comprising:

a step of forming a first substrate 401, the first substrate 401 having a semiconductor region and an insulating region 402 on a surface thereof, figs. 7+,

a step of coating the first substrate with a single-crystal semiconductor layer 404, col. 5, lines 1+,

wherein in the coating step, a single-crystal semiconductor is longitudinally grown in the semiconductor region and then laterally grown.

Art Unit: 2812

Takasu et al. teaches a substrate manufacturing method comprising:

a step of forming a first substrate 2, the first substrate 2 having a semiconductor region and an insulating region 4 on a surface thereof, figs. 2D,

a step of coating the first substrate with a single-crystal semiconductor layer 16, col. 3, lines 58+,

wherein in the coating step, a single-crystal (monocrystal) semiconductor is longitudinally grown (about 1-4 μm) in the semiconductor region and then laterally grown (about 1 μm).

or

a step of coating the first substrate with a single-crystal semiconductor layer 16/22, col. 4, lines 35+,

wherein in the coating step, a single-crystal semiconductor is longitudinally grown.

Koide et al. teaches a substrate manufacturing method comprising:

a step of forming a first substrate 10, the first substrate 10 having a semiconductor region and an insulating region 18 on a surface thereof, figs. 5A,

a step of coating the first substrate 10 with a single-crystal semiconductor layer 20, col. 8, lines 15+,

wherein in the coating step, a single-crystal semiconductor 20 is longitudinally grown in the semiconductor region and then laterally grown,

Art Unit: 2812

polishing (planarizing) semiconductor layer 18, 20, 22, col. 6, lines 55+, col. 9, lines 8+.

The difference between the references applied above and the instant claim(s) is: Nishida et al. or Takasu teaches forming a single crystalline layer but does not teach a bonding and using insulating layer as separation layer. However, Short et al. teaches at figures 11-20 and col. 4, lines 61+ and col. 5, lines 7+ that a bonding (handling) wafer 30 to the first substrate 10 with a single crystalline layer 15 and forming a separation layer 35 and separating the bonded substrate at the separation layer 35 (col. 6, lines 20+) and polishing (planarized) the single crystalline layer 15 (col. 4, lines 30-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with a bonding wafer and a separation layer as taught by Shorts because semiconductor devices can be formed on the single crystalline layer that is formed on the insulating layer so that the current leakage in the device will be minimized.

Conclusions

Applicant's arguments filed on Oct. 25, 2004 have been fully considered but they are not persuasive. Because Short et al. clearly teaches Short et al. teaches at figures 11-20 and col. 4, lines 61+ and col. 5, lines 7+ that a bonding (handling) wafer 30 to the first substrate 10 with a single crystalline layer 15 and forming a separation layer 35 and separating the bonded substrate at the separation layer 35 (col. 6, lines 20+) and polishing (planarized) the single crystalline layer 15 (col. 4, lines 30-60). It would have been obvious to one of ordinary skill in the art to bond two wafers having a single

Art Unit: 2812

crystalline layer and thinning one of the wafer to form an SOI substrate for forming semiconductor device to improve the leakage characteristics.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is (703) 308-4357.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679.

The fax phone number for this Group is (703) 872-9306.

hjt

12/11/04



H. Jey Tsai
Primary Examiner
Patent Examining Group 2800

FORM PTO 1449 (modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE LIST OF REFERENCES CITED BY APPLICANT(S) (Use several sheets if necessary)				ATTY DOCKET NO. 00862.023223		APPLICATION NO. 10/654,022	
<div style="border: 2px solid black; border-radius: 50%; padding: 10px; display: inline-block;"> OPEN JC139 SEP 03 2004 PATENT & TRADEMARK OFFICE </div>				APPLICANT NOBUHIKO SATO ET AL.			
				FILING DATE September 4, 2003		GROUP 2812	
U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
M		3,372,063	03/05/68	Suzuki et al.	438	413	
		4,498,951	02/12/85	Tamura et al.	117	43	
		4,459,926	10/29/85	Corboy, Jr. et al.	438	412	
		4,585,493	04/29/86	Anthony	117	42	
		4,725,561	02/16/88	Haond et al.	438	404	
		4,874,718	10/17/89	Inoue	438	481	
		4,952,526	08/28/90	Pribat et al.	438	412	
M		5,084,419	01/28/92	Sakao	438	400	
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/ OR ABSTRACT
M	EP	1 100 124 A1	05/16/01	Europe			
OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER		H. Jay T... <i>H. Jay T...</i>			DATE CONSIDERED		
					12/1/04 <i>12/1/04</i>		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
<i>W</i>		5,086,011	02/04/92	Shiota	438	406	X	
<i>W</i>		5,397,735	03/14/95	Marcandalli et al.	438	459		
<i>W</i>		5,945,703	08/31/99	Furukawa et al.	257	301		
<i>W</i>		6,562,692 B1	05/13/03	Oi et al.	438	406		
<i>W</i>		2004/0033674 A1	02/19/04	Todd	438	478		08/14/02
<i>W</i>		2004/0058511 A1	03/25/04	Sakaguchi	438	458		09/04/03
FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/ OR ABSTRACT	
OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)								
EXAMINER		<i>H. Ser T. M.</i>			DATE CONSIDERED <i>12/11/04</i>			

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Sheet 2 of 2